TESTING ACTIVITIES IN PARIS

DAMIC kick off meeting
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Romain Gaïor (LPNHE Paris) for the Paris Group

Hardware: H. Lebbolo, L. Khalil, M. Dhelot.
Firmware: D. Martin
Software: P. Bailly, Z. Wang
ACTIVITIES IN PARIS

CCD

Flex cable

Clock

Signal

Clock / Bias Generation

DC power

Amplification
CDS

Numeric Conversion (ADC)

DAQ Control

CABAC

18 bits 15 MS/s board
(see Latifa's talk)
ASPIC

- ASIC developed for LSST
  - Programmable gain 1 to 13
  - On chip DSI (Dual Slope Integrator) max RC = 4us
ASPIC: TEST BENCH

CCD Frame Adapter

ASPIC

*Cyclone 3 eval board  DK-DEV-3C120N*
ASPIC: SOME RESULTS

Test in Paris
• Amplitude evolution with time
• Noise measurements

Tests at U of Chicago
• Used ASPIC with a Leach system and a CCD
• Minimum noise of 5 e⁻
CABAC

- ASIC developed for LSST
- Programmable output clocks, adjustable slopes
- DAMIC CCD require more clocks and Bias —> 3CABAC
- Add on board to test the clocks
ASPIC + CABAC: TEST BENCH

3CABAC  FPGA  ADC  ASPIC

• Requires a set of adjustment in hardware/firmware/software
• First time these solutions work together
ASPIC + CABAC: SOFTWARE
ASPIC + CABAC: FIRST TEST

- hypothetical 4 lines x 8 column CCD
- Set all the required clocks
- Will test with a CCD in the next weeks
NEXT STEPS

- Test of read out and clocking integrated solutions (ASPIC and CABAC) with a CCD
- Design a similar test bench for CROC
- Compare it with existing solutions (test bench equipped with a Leach)
Back up
DAQ and control

Carte IDROGEN

- On board configuration (µC)
- Very low noise synthesizer PLL synthesizer cleaner (LM04828) for WR clk and derived clk.
- Dedicated PLL for serial links
- Integrated USBBlaster II.
- FPGA configuration: Active serial, IP bus.
- External connectivity: PPS, Trigger, Ext CLK.
Commentaires:
CKP3 cabac1 point test
CKP123 cabac2 points tests
CKP3 cabac3 point test
CKP0123 cabac3 points test
KS2 et RG cabac3 points test

LVDS CLOCK Cab1
- MOSI, NRESET, SCLK, NSS CAB1, RO Cab1
  - D590C031B CMOS TO LVDS
  - SN74AVC4T245 3.3V TO 2.5V

LVDS CLOCK Cab1
- MOSI, NRESET, SCLK, NSS CAB1, RO Cab1
  - Cabac #1 +40V/BGND
    - D590C031B CMOS TO LVDS
    - SN74LVCC3245a 2.5V TO 3.3V
    - OPA547 Suiveur +10V & BGND

LVDS CLOCK Cab2
- MOSI, NRESET, SCLK, NSS CAB1, RO Cab2
  - Cabac #2 +40V/BGND
    - D590C031B CMOS TO LVDS
    - SN74LVCC3245a 2.5V TO 3.3V
    - OPA547 Suiveur +10V & BGND

LVDS CLOCK Cab2
- MOSI, NRESET, SCLK, NSS CAB1, RO Cab2
  - Cabac #3 +40V/BGND
    - D590C031B CMOS TO LVDS
    - SN74LVCC3245a 2.5V TO 3.3V
    - OPA547 Suiveur +10V & BGND

VDD_U
- 10 ohms au BGND

Con 160p
- SAMTEC HSMC

Con 50p