

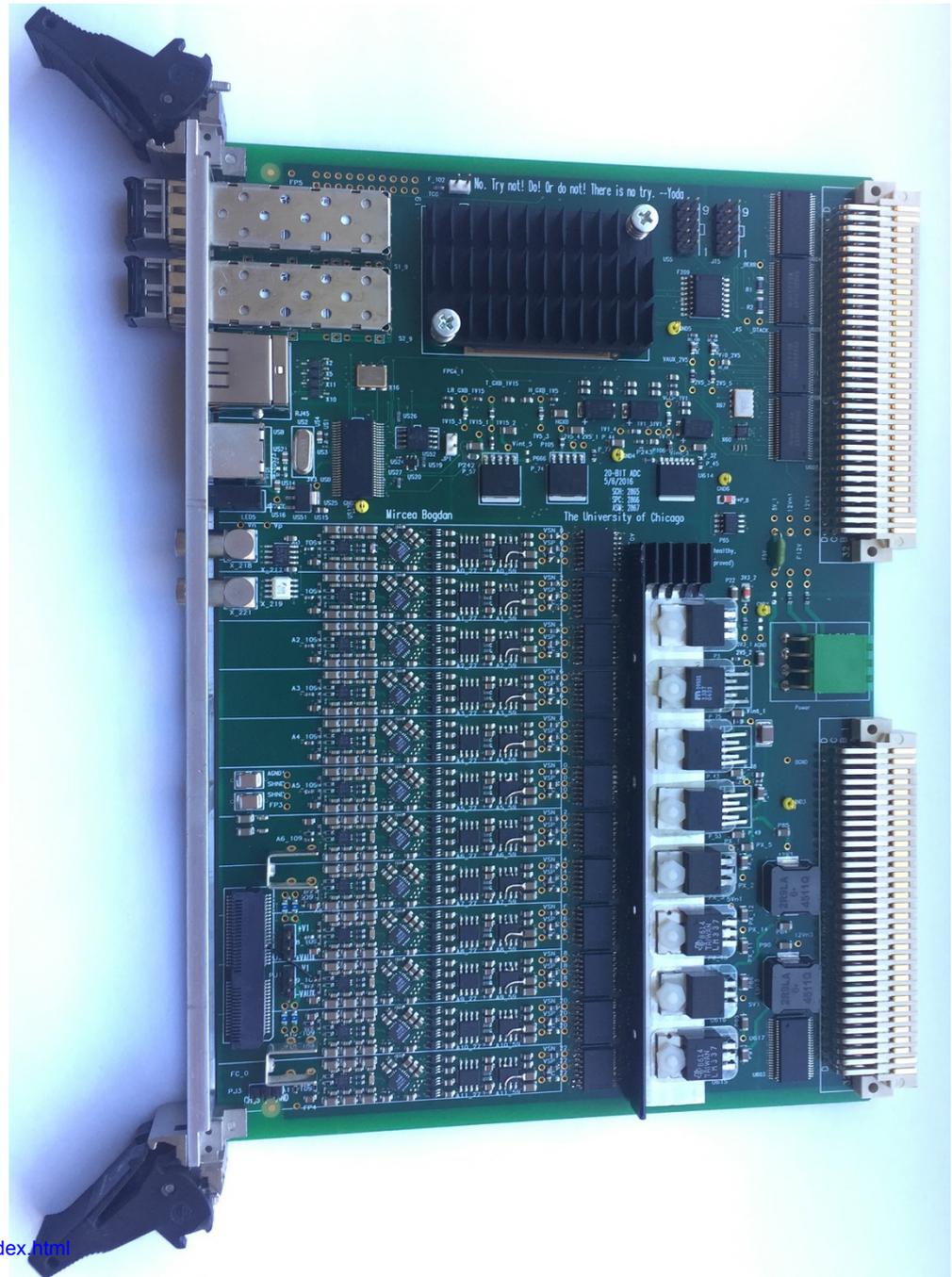
# 20-BIT ADC Module

Mircea Bogdan  
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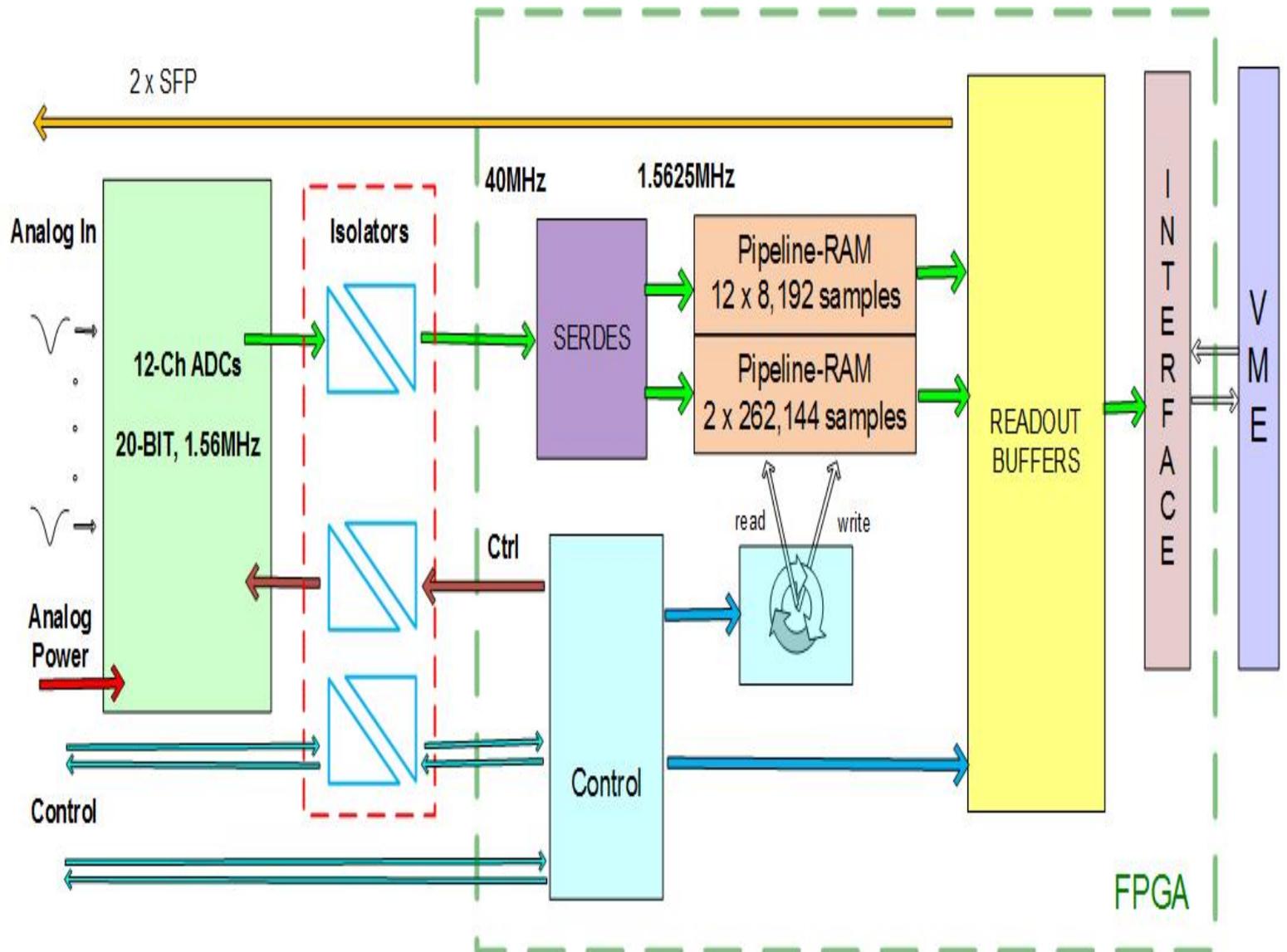
The University of Chicago

# 20-BIT ADC

## Prototype



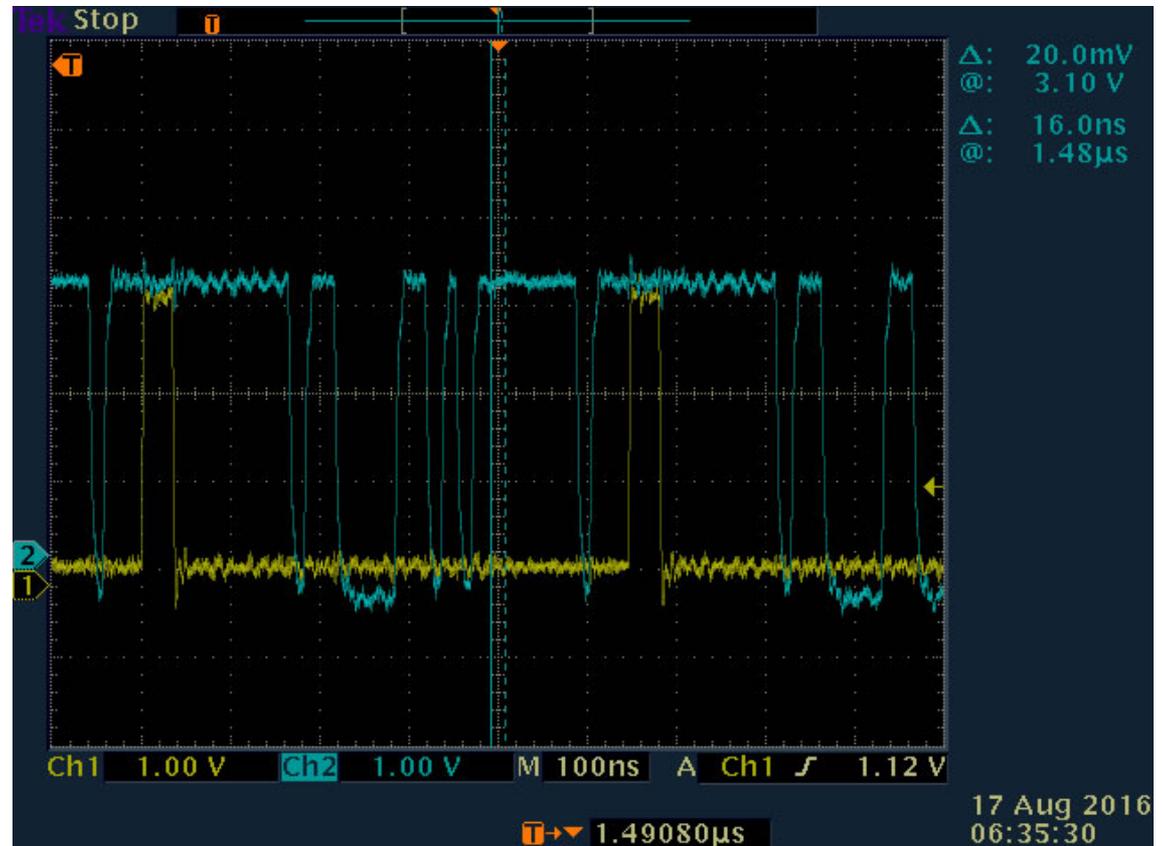
# 20-BIT ADC Block Diagram



# 20-BIT ADC Readout

## 12 ADC Channels:

- 1.6MHz Sampling
- 50Mhz serial Readout



# Noise Levels for the 12 ADC Channels

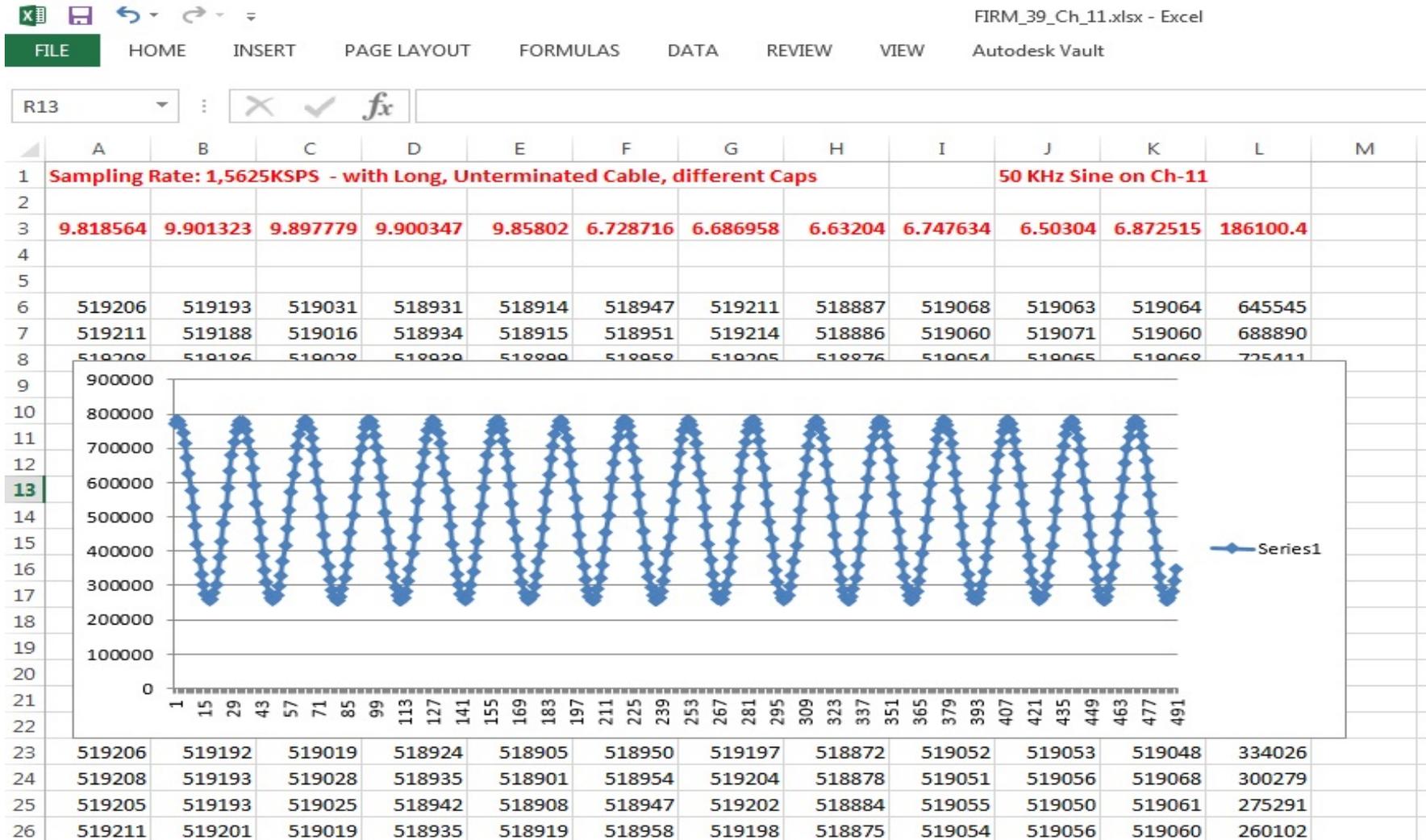
FIRM\_39\_NOISE\_1.xlsx - Excel

FILE HOME INSERT PAGE LAYOUT FORMULAS DATA REVIEW VIEW Autodesk Vault

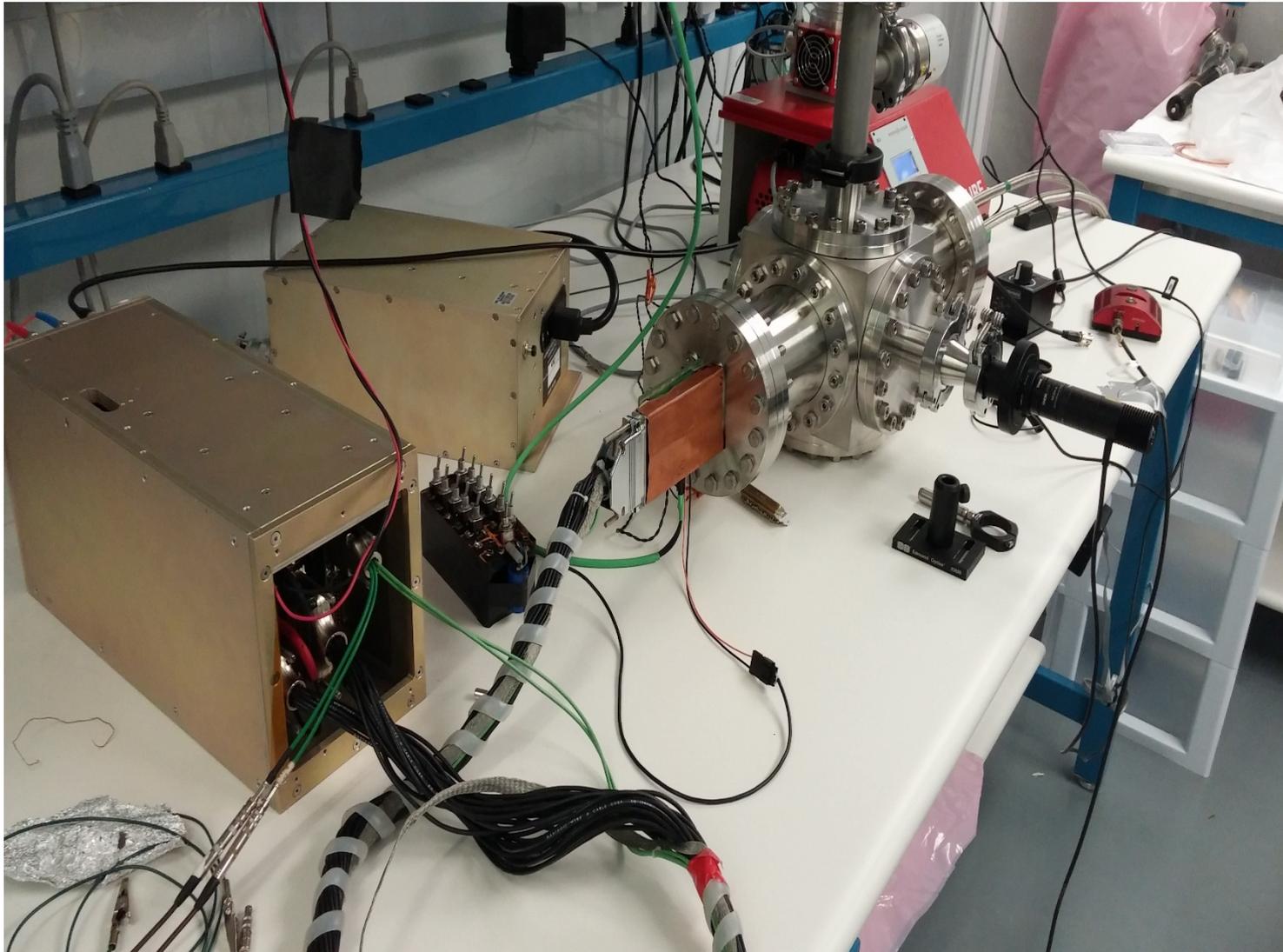
L3 :   *fx* =STDEV(L6:L5001)

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Sampling Rate: 1,5625KSPS - with NO Cable												
2													
3	4.495533	4.610118	4.809599	4.681379	4.517198	4.480513	4.366816	4.323622	4.290939	4.37509	4.4202	4.338324	
4													
5													
6	519201	519193	519012	518921	518902	518940	519203	518875	519047	519062	519062	518800	
7	519206	519192	519022	518932	518907	518947	519202	518891	519051	519057	519071	518806	
8	519205	519193	519016	518920	518917	518950	519197	518884	519058	519056	519061	518808	
9	519203	519192	519020	518940	518904	518953	519199	518876	519053	519058	519064	518810	
10	519211	519192	519014	518917	518904	518950	519198	518880	519062	519064	519064	518807	
11	519208	519189	519016	518923	518900	518953	519201	518879	519049	519054	519064	518804	
12	519207	519188	519019	518924	518904	518946	519195	518865	519047	519058	519068	518810	
13	519197	519188	519021	518932	518908	518950	519208	518872	519058	519059	519068	518803	
14	519201	519194	519016	518932	518904	518957	519202	518875	519051	519057	519067	518801	
15	519210	519191	519015	518922	518911	518953	519201	518886	519048	519062	519059	518799	
16	519201	519190	519029	518934	518907	518950	519202	518876	519053	519058	519062	518809	
17	519202	519187	519012	518930	518905	518952	519202	518880	519054	519055	519065	518804	
18	519198	519195	519014	518935	518909	518949	519200	518876	519055	519057	519061	518812	
19	519207	519194	519016	518931	518913	518948	519203	518877	519051	519057	519057	518807	

# 20-BIT ADC Signal



# Test Setting in Chicago



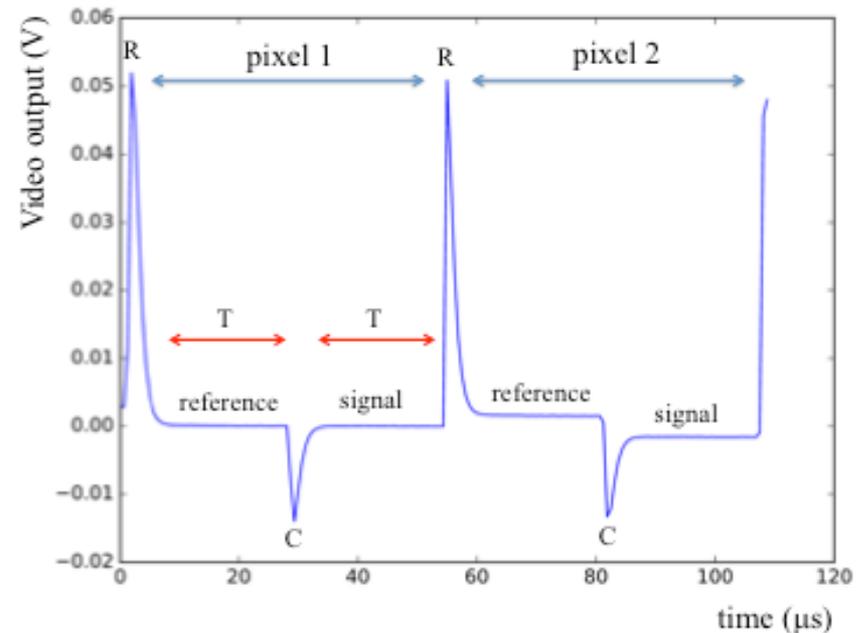
# 20-BIT ADC - Testing

- The ADC module was integrated with a CCD and Controller (Leach) in Chicago.
- The ADC board itself was placed in a 21-Slot Wiener UEP 6021 VME crate.
- External power to the analog front-end components - Keysight 3631A DC power supply.
- The CCD: LBNL 2k by 4k 500 micrometer thick fully-depleted p-channel thinned back-illuminated CCD.
- The video signal from the CCD - through a custom second-stage interface board and an inverting board
- Clock signals for the CCD itself were provided by the Leach.
- Additional testing of bandwidth and crosstalk with an Agilent 33120A Function Generator.
- Interface with the ADC module via an Abaco 7865RC VME controller, with custom C++ code.
- Crosstalk: 6Vpp sine into one channel and measure amplitude in other channels from 1 to 800 kHz.
- The maximum crosstalk observed was -66.6dB at 400 kHz.
- Noise was measured using sets of 8,192 samples at a time
- The ADC module itself with VME readout showed an Equivalent Input Noise of about 4.5LSB-RMS, corresponding to a Signal-to-Noise Ratio of 98.7dB. With floating or grounded inputs, no deviation from white noise was observed.
- When integrated with the CCD and readout chain, the noise increased to 10 LSBs, with significant 1/f noise with a corner frequency of 100 kHz, due to the CCD amplifier chain.

# 20-BIT ADC - Conclusions

We have successfully developed a prototype 20-bit ADC for the CCD readout. The ADC is routinely used to take CCD images at UChicago. The readout noise level is  $2 e^-$ , similar to that of the Leach and Monsoon

Example of CCD trace by the 20-bit ADC



We will work on the integration in the DAMIC-M electronics of the experience gained with this design