Electronics for DAMIC-M

DAMIC-M kick-off meeting
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Electronics for DAMIC-M

• CCD Readout
  – Requirements
  – From DAMIC 100 to DAMIC-M
  – From ASPIC to CROC

• CCD Control
  – CABAC
  – New ASIC?

• Readout and Control board : ODILE
CCD readout : Requirements

• 4 channels, single ended in, differential out
• Work near the CCD at 140K (no packaging)
• Gain :
  
  CCD response is \(\sim 2.5\mu V/e^-\), full well is \(\sim 75ke^-\), ADC input swing is 6 or 8V.
  If we want to read full well, gain must be \(\sim 32\)
  If max event is \(\sim 15ke^-\), gain must be \(\sim 160\)
    \(\Rightarrow\) Programmable gain

• Noise :
  
  – Target is \(0.2e^-\), \((0.5\mu V)\)
  – Bandwidth : \(\sim 1MHz\)

• Read out :
  
  – Oversampled & digital filtered transparent mode (clamp & sample)
  – Dual Slope Integrator (oversampled or not)
From DAMIC 100 to DAMIC-M

• DAMIC 100 readout is DSI
  – Overall Gain \( G = A \times T/RC \)
  \( A \) : first stage gain, \( T \) : integration time, \( RC \) : integrator time constant

• Gain topology is not optimum for noise

• For best noise performance :
  – \( A \) must be maximum
  – \( T/RC \sim 1 \)

CCD + jFet + gain 2 amp
Amplifier \( G=16 \)
DSI
RC = 260ns
T ~ 20µs
ADC 18b
Overall gain $G=500$  \quad Integration time $T=25\mu s$

$A = 10$ , $RC = 500$ns  \quad $\Rightarrow$  \quad RMS noise $=9.1\mu V$
Overall gain $G=500$  
Integration time $T=25\mu s$

$A = 100$ , $RC = 5\mu s$  $\Rightarrow$  RMS noise $= 0.91\mu V$
FROM ASPIC to CROC

• **ASPIC** (Analogue Signal Processing IC) has been developed for LSST
  – 8 channels
  – Max gain: 13, max RC ~4µs
  – ASPIC is not optimized for DAMIC

• **CROC** (CCD ReadOut Chip)
  – Programmable gain up to 128 (first stage)
  – Programmable RC from 200ns to 50µs
**CCD clocking and biasing**

- **CCD needs many clocks:**
  - Vertical (Parallel) to move lines: 3 clocks + TG
    - 2 sets needed to move one half up & 2nd down
    - Current capability: \( \Delta V=8V, \, tr=2\mu s, \, C=100nF \rightarrow I=400mA \)
  - Horizontal (Serial) to move pixels: 3 clocks
    - 2 sets needed to move one half right & 2nd left
    - Low current capability
  - Reset Gate, Summing well + Skipper clocks

- **Power supply & Biases:**
  - Vdd (Output Drain) ~1mA each
  - Vreset (Reset Drain)
  - OG
  - Skipper CCD biases
CABAC: clocks and biases

- Provide:
  - Parallel and serial clocks; Reset Gate
  - CCD biases (OG, RD (=VR), GD, spare)
  - CCD amplifier power supply OD (=VDD)
  - Clocks & biases multiplexer for debugging purpose
  - Temperature sensor
  - Electronic calibration pulser
  - Can be translated wrt local ground to comply with CCD type
  - Techno CMOS 0.35µ HV
Parallel clocks

DAC : 255
Total load : 66nF
Amplitude : 9V
X talk ~400mV
Serial clocks

DAC : 255
Total load : 200pF
VDD_U : 5V
VDD_L : -4V
CABAC on DAMIC

- Board with 3 CABAC to control one CCD has been developed
- Programmable (10 bit) rails for clocks
- Programmable clocks current capability (slope)
- Programmable biases level (10 bit)
- Clocks triggered by lvds signals sent by FPGA
- Possibility to generate CCD Vsub
- Programmation done by SPI bus
- Board is tested, firmware and software to generate biases and clocks work
- Board will be used on one of our test bench
New CCD control ASIC?

- Modify CABAC with current sink biases capability
- Generation of programmable Clocks rails
- Increase the number of clocks
Readout & Control : ODILE

- ODILE : Online Digital Interface for Low noise Electronics
- Modular system : one board for one CCD
- Can be used as a single CCD camera readout & control
- One mother board with data link to the DAQ
  - One 4 channels readout daughter board
  - One CCD control daughter board
ODILE simplified synoptic

4 channels ADC board

Video data

FPGA

One CCD control board

Video

CCD + CROC

CROC prog & timing
CCD clock & biases

ADC timing

R & C prog
CCD timing
CROC timing

Central DAQ
ODILE mother board

• IDROGEN : IN2P3 open project of generic DAQ with FMC connector for specific application
  • Optical link up to 40Gb/s
  • Located in Xtca crate
  • Not enough onboard space for Damic application

• New FPGA evaluation board with onboard memory and 2 connectors for control & readout
Next step: CROC tests

- FPGA evaluation board with at least one dedicated connector
- One 4 channels ADC board
- Room temp CROC test board
  - Bounded CROC
  - Packaged CROC, clamshell support
- Cryo temp tests: CROC bounded on a board connected to CCD